In the Claims:

1. (Currently Amended) A method of forming a trench isolated integrated circuit device comprising:

forming a trench including sidewalls in an integrated circuit substrate;

forming a lower device isolation layer in the trench and extending onto the trench sidewalls, the lower device isolation layer including long, narrow grooves therein, a respective one of which extends along a respective one of the sidewalls, such that a respective groove spaces apart the lower device isolation layer adjacent thereto, from a respective sidewall; and

forming an upper device isolation layer on the lower device isolation layer and in the grooves.

2. (Currently Amended) A method according to Claim 1 wherein the forming a lower device isolation layer comprises:

forming a conformal liner layer on the sidewalls;

forming a lower device insulation layer on the conformal liner layer; and

etching the conformal liner layer to recess the conformal liner layer relative to the lower device insulation layer adjacent thereto, to thereby define the long, narrow grooves that space apart the lower device isolation layer adjacent thereto, from the respective sidewall.

3. (Original) A method according to Claim 2 wherein the forming a lower device insulation layer comprises:

forming a first insulation layer on the conformal liner layer; and

forming a second insulation layer on the first insulation layer.

4. (Original) A method according to Claim 1:

wherein the forming a trench is preceded by forming a buffer insulation layer and a hard mask layer on the integrated circuit substrate;

wherein the forming a trench comprises forming an opening in the hard mask layer and in the buffer layer to expose the integrated circuit substrate and forming the trench in the integrated circuit substrate that is exposed by the opening;

wherein the forming an upper device isolation layer comprises forming an upper device isolation layer on the lower device isolation layer, in the grooves and in the opening; and

wherein the forming an upper device isolation layer is followed by removing the hard mask layer and the buffer insulation layer.

5. (Original) A method according to Claim 1 wherein the following is performed between the forming a trench and the forming a lower device isolation layer:

forming a sidewall oxide layer on the sidewalls.

6. (Original) A method according to Claim 1 further comprising;

forming a plurality of transistors on the trench isolated integrated circuit device.

7-10. (Canceled)

11. (Currently Amended) A method of forming an integrated circuit, comprising:

sequentially forming a buffer insulation layer and a hard mask layer on a substrate face;

successively patterning the hard mask layer and the buffer insulation layer to form an opening that exposes a predetermined region of the substrate;

selectively etching the predetermined region of the substrate to form a trench including a floor and sidewalls;

forming a lower device isolation layer including long, narrow grooves within the trench, wherein the grooves are disposed adjacent the sidewalls remote from the floor, such that a respective groove spaces apart the lower device isolation layer adjacent thereto, from a respective sidewall;

forming an upper device isolation layer on the lower device isolation layer to fill the grooves and the trench; and

etching the hard mask layer and the buffer insulation layer, such that the

grooves extend a predetermined depth from the substrate face.

12. (Original) A method of Claim 11, wherein the forming a lower device isolation layer is preceded by forming a sidewall oxide layer on the sidewalls and the floor.

13. (Currently Amended) A method of Claim 11, wherein the forming the lower device isolation layer comprises:

forming a conformal liner layer on the substrate face and in the trench;

forming a lower device insulation layer on the liner layer and in the trench;

isotropically etching the lower device insulation layer until the liner layer in the opening is exposed, to form a lower device insulation pattern in the trench; and

isotropically etching the liner layer to form a liner in the trench, wherein edges of the liner are recessed a predetermined depth from the substrate face to define the long, narrow groove that spaces apart the lower device isolation layer adjacent thereto, from the respective sidewall.

14. (Original) A method of Claim 13, further comprising forming a conformal etch protection layer on the conformal liner layer prior to forming the lower device insulation layer.

15. (Original) A method of Claim 13, wherein the lower device insulation layer comprises at least two supplementary insulation layers that are stacked.

16. (Original) A method of Claim 11, wherein the forming the upper device isolation layer comprises:

forming an upper device insulation layer on the substrate face and on the lower device isolation layer to fill the grooves and the trench; and

planarizing the upper device insulation layer until the hard mask layer is exposed, to form the upper device isolation layer.

17. (Original) A method of Claim 16, wherein the forming the upper

device insulation layer is preceded by conformally forming a capping insulation layer to fill the groove, wherein the capping insulation layer comprises insulation material having etch selectivity with respect to the hard mask layer.

18. (Original) A method of Claim 11:

wherein the sequentially forming comprises sequentially forming a tunnel insulation layer, a first floating gate conductive layer, a buffer insulation layer, and a hard mask layer on a substrate face;

wherein the successively pattering comprises successively patterning the hard mask layer, the buffer insulation layer, the first floating gate conductive layer, and the tunnel insulation layer to form a first floating gate pattern and an opening that exposes a predetermined region of the substrate; and

wherein the etching comprises etching the hard mask layer and the buffer insulation layer until the first floating gate pattern is exposed.

19. (Original) The method of Claim 18, further comprising:

forming a second floating gate pattern on the first floating gate pattern;

sequentially forming a dielectric layer and a control gate conductive layer on the substrate face and the second floating gate pattern; and

successively etching the control gate conductive layer, the dielectric layer, the second floating gate pattern and the first floating gate pattern to form a first floating gate electrode, a second floating gate electrode, a dielectric pattern and a control gate electrode.

20. (Original) A method according to Claim 11 further comprising:

forming a plurality of transistors on the substrate face.